MEMS Deformable Mirror Development for Space-Based Exoplanet Detection

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Approved for public release; unlimited distribution
Iris AO Segmented DM
Background
Iris AO MEMS Segmented Deformable Mirrors

PTT111 DM
- 111 Actuators
- 37 PTT Segments
- 3.5 mm inscribed aperture
- Factory calibrated

PTT489 DM
- 489 Actuators
- 163 PTT Segments
- 7.7 mm inscribed aperture
- Factory calibrated
Iris AO Segmented DM Background

- **3 DOF**: Piston/tip/tilt electrostatic actuation – no hysteresis
- **Hybrid fabrication process**
  - 3-layer polysilicon surface micromachining
  - Single-crystal-silicon assembled mirror
- **Unit cell easily tiled to create large arrays**
- **Hybrid technology**
  - Thick mirror segments
  - <1 nm PV/°C segment bow
  - Enables back-side stress-compensation coatings

![Diagram of Iris AO Segmented DM Background](image)
Hybrid Fabrication Process

a) AuSiO2/TEOS CrSi
b) Chip-scale thermo-compresion flip-chip bond

Mirror-aperture clearing etch

Microstructure release and optical coating
NASA Application

Visible Nulling Coronagraph (VNC)
Exoplanet Imaging Requirements: VNC Technology

- Usable Dynamic Range (Stroke): $1.0 \mu m$
- Segment Control Resolution: $15 \text{ pm} \ rms$
  - ATLAST: may now be $1 \text{ pm} \ rms$
- ~1000 Segment DM
- Segment Flatness: 1-3 nm $\text{rms}$


$10^9$ Contrast @ IWA 1 – 4 $\lambda/D$ Results GSFC VNC Instrument on 06/09/12
Phase II SBIR Development

Critical Development for Manufacturing DMs for Exoplanet Detection
Phase II Objectives

NNX11CE94P
• Improve DM quality
  – Improve segment flatness for entire array
  – Reduce chip bow
  – Increase segment position uniformity
• Scale technology to 1000-actuator DM
  – Increase yield
  – Demonstrate PTT939 array
• Demonstrate pm-level positioning
  – 15 pm rms

NNX14CG06C
• Wafer Scale DM Assembly
• 16 Bit Electronics
• Hardware-based super resolution electronics controller
# Mirror-Segment-Flatness Improvements

<table>
<thead>
<tr>
<th>Segment Design</th>
<th>Average $rms$ Errors</th>
<th>Worst $rms$ Errors</th>
</tr>
</thead>
<tbody>
<tr>
<td>25 µm</td>
<td>12</td>
<td>22</td>
</tr>
<tr>
<td>50 µm</td>
<td>3</td>
<td>4.5</td>
</tr>
<tr>
<td>50 µm (400 µm Aperture)</td>
<td>1.5 (1.1, best result)</td>
<td>2.1</td>
</tr>
<tr>
<td>25 µm Optimized</td>
<td>5</td>
<td>8</td>
</tr>
<tr>
<td>50 µm Optimized</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

- Matches 1st Order Theory Well: 4X reduction for 50 µm vs. 25 µm segments
- Phase II Goal: 2 nm $rms$
- If trends hold, ~1.25 nm $rms$ over entire segment should be possible

## 50 µm-Thick DM Segments - Phase II Deliverable

### Full Aperture (10 µm Exclusion)

### Partial Aperture (400 µm Aperture)

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Unpowered DM Figure Improvement

Unpowered PTT489 DM

Pre Phase II

Phase II Interim Deliverable
DM Packaging Improvements

• Reduced mass
  – 1.26 kg → 0.34 kg
• Reduced footprint
  – 5”x10” → 2”x5.5”
• Increased Thermal Stability (nm PV/°C)
  – 12.5 → 3.5

<table>
<thead>
<tr>
<th>Description</th>
<th>Weight (oz)</th>
<th>Mass (kg)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PGA Package</td>
<td>1.9</td>
<td>0.05</td>
</tr>
<tr>
<td>MIB PCB</td>
<td>13.0</td>
<td>0.37</td>
</tr>
<tr>
<td>Mounting Block</td>
<td>29.6</td>
<td>0.84</td>
</tr>
<tr>
<td><strong>Total (summed)</strong></td>
<td><strong>44.5</strong></td>
<td><strong>1.26</strong></td>
</tr>
<tr>
<td><strong>Total (measured)</strong></td>
<td><strong>44.5</strong></td>
<td><strong>1.26</strong></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Description</th>
<th>Weight (oz)</th>
<th>Mass (kg)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LGA Package</td>
<td>3.0</td>
<td>0.09</td>
</tr>
<tr>
<td>Enclosure Top</td>
<td>2.5</td>
<td>0.07</td>
</tr>
<tr>
<td>Enclosure Base</td>
<td>3</td>
<td>0.09</td>
</tr>
<tr>
<td>Mounting Bracket</td>
<td>3.2</td>
<td>0.09</td>
</tr>
<tr>
<td><strong>Total (summed)</strong></td>
<td><strong>11.7</strong></td>
<td><strong>0.33</strong></td>
</tr>
<tr>
<td><strong>Total (measured)</strong></td>
<td><strong>11.8</strong></td>
<td><strong>0.34</strong></td>
</tr>
</tbody>
</table>
### DM Yield

<table>
<thead>
<tr>
<th>Build Number</th>
<th>Actuator</th>
<th>Wafer Lot</th>
<th>Mirror Wafer Lot</th>
<th>Electrical Segment Yield</th>
<th>Total Segment Yield</th>
<th>Chip Yield</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PWA-02</td>
<td>LSM-01</td>
<td>66.8%</td>
<td>83.4%</td>
<td>55.7%</td>
<td>0.0%</td>
</tr>
<tr>
<td>2</td>
<td>PWA-02</td>
<td>LSM-02</td>
<td>93.9%</td>
<td>92.4%</td>
<td>86.8%</td>
<td>0.0%</td>
</tr>
<tr>
<td>3</td>
<td>PWA-03</td>
<td>LSM-02</td>
<td>97.6%</td>
<td>98.8%</td>
<td>96.8%</td>
<td>18.8%</td>
</tr>
<tr>
<td>4</td>
<td>PWA-03</td>
<td>LSM-02</td>
<td>98.8%</td>
<td>99.1%</td>
<td>96.5%</td>
<td>20.0%</td>
</tr>
<tr>
<td>5</td>
<td>PWA-03</td>
<td>LSM-02</td>
<td>98.3%</td>
<td>98.7%</td>
<td>97.3%</td>
<td>28.6%</td>
</tr>
<tr>
<td>6</td>
<td>PWA-04</td>
<td>LSM-02</td>
<td>99.4%</td>
<td>97.8%</td>
<td>97.2%</td>
<td>0.0%</td>
</tr>
<tr>
<td>7</td>
<td>PWA-05</td>
<td>LSM-03</td>
<td>TBD</td>
<td>TBD</td>
<td>TBD</td>
<td>TBD</td>
</tr>
</tbody>
</table>

- Ideally yield increases monotonically with every fabrication lot
- Defects in contact masks increased electrical failures for PWA-04 actuator lot
  - Defects were more uniformly distributed rather than clustered
  - Result: 0% chip yield
- Goal: fully functional PTT939 DM
- PWA-05 Run
  - New masks
- PTT939 DM will use DUV stepper photolithography
  - Fewer defects from lithography

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NASA Phase II SBIR: Remaining Work

- NNX11CE94P
- Demonstrate PTT939 DM
  - Transition fabrication process to DUV stepper lithography system
- Demonstrate mass-reduced DM segments on a PTT489
  - Phase IIE
Electronics Development

• Existing Iris AO Drive Electronics are 14-bit resolution

NNX14CG06C Development
• 16-bit resolution HV driver card
  – Card built and preliminarily tested

• USB2.0 High Speed Interface
  – Microcontroller
  – FPGA to implement timing critical modulation
  – Windows and Linux compatible
  – Built, tested, and currently being incorporated into Iris AO interface software
High-Resolution Drive Electronics

• pm $rms$ level control will require >20 bit electronics
  – 2 µm stroke DM, 1 µm stroke after flattening
  – Nonlinearity in MEMS electrostatic actuation reduces resolution

• State-of-the art HV MEMS Drivers are 14-16 bit resolution

• Signal processing techniques can be used to increase resolution (super resolution)
  – NASA New Technology Report to be filed
Super-Resolution Drive Electronics

- Electronics are 14 bit resolution
- Grid spacing is for 1 LSB on 18 bit resolution
- Super-resolution demonstration
  - +4 bits were demonstrated
- FPGA controlled signals will provide even better resolution

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Scaling Up: Wafer-Scale Assembly

- DMs >1000 actuators require wafer-scaled assembly techniques
- Phase I demonstrate a scalable bonding technique using a eutectic bond
- Recent increased bond-tool tool capacity and process optimization enables wafer-scale thermo-compression
  - gives a lower risk path to wafer-scale assembly
- Eutectic bond will be developed as a back up plan
Summary

Technologies developed to produce DMs capable of meeting VNC requirements

• Segment flatness 2nm $rms$ over VNC subapertures
  – Path to flatter segments
• Segment position variations reduced to suitable levels for testbed environment
• Compact, more thermally stable packaging
• Major yield improvements
  – Defects on recent PEA-04 run determined
  – Higher yields expected on PWA-05 run
• Demonstrated means to reach 20 bit drive electronics resolution
• Wafer-scale assembly under development
  – Enables scaling to 4th generation 1000 segment (3000 actuator) DM
• Design of 3rd generation 1000 actuator DM underway